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# NC7SZ66

## Low Voltage Single SPST Normally Open Bus Switch

### Features

- Broad  $V_{CC}$  Operating Range: 1.65 V to 5.5 V
- Rail-to-Rail Signal Handling
- Power Down High-Impedance Inputs/Outputs
- 5  $\Omega$  Switch Connection between Two Ports
- Minimal Propagation Delay through the Switch
- Low  $I_{CC}$
- Zero Bounce in Flow-Through Mode
- Control Input Compatible with CMOS Input Levels
- Ultra-Small MicroPak™ Packages
- Space-Saving SOT23 and SC70 Packages

### Description

The NC7SZ66 is a ultra high-speed (UHS) CMOS compatible single-pole/single-throw (SPST) bus switch. The LOW on resistance of the switch allows inputs to be connected to outputs with minimal propagation delay and without generating additional ground bounce noise. The device is organized as a 1-bit switch with a switch enable (OE) signal. When OE is HIGH, the switch is on and port A is connected to port B. When OE is LOW, the switch is open and a high-impedance state exists between the two ports..

### Ordering Information

Part Number	Top Mark	Package	Packing Method
NC7SZ66M5X	7Z66	5-Lead SOT23, JEDEC MO-178 1.6 mm	3000 Units on Tape & Reel
NC7SZ66P5X	Z66	5-Lead SC70, EIAJ SC-88a, 1.25 mm Wide	3000 Units on Tape & Reel
NC7SZ66L6X	EE	6-Lead, MicroPak™, 1x1 mm Wide	5000 Units on Tape & Reel

## Connection Diagrams



Figure 1. Logic Symbol

## Pin Configurations

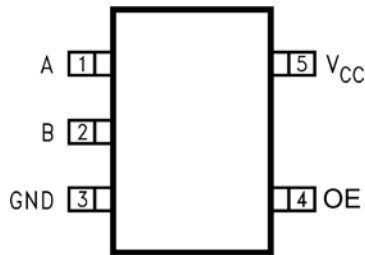


Figure 2. SC70 and SOT23 (Top View)



Figure 3. MicroPak™ (Top Through View)

## Pin Definitions

Pin # SC70 / SOT23	Pin # MicroPak™	Name	Description
1	1	A	Bus A I/O
2	2	B	Bus B I/O
3	3	GND	Ground
4	4	OE	Switch Enable Input
5	6	V <sub>CC</sub>	Supply Voltage
	5	NC	No Connect

## Function Table

OE	B <sub>0</sub>	Function
L	High Z-State	Disconnected
H	A <sub>0</sub>	Connect

H = HIGH Logic Level

L = LOW Logic Level

## Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only.

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply Voltage	-0.5	7.0	V
$V_S$	DC Switch Voltage <sup>(1)</sup>	-0.5	$V_{CC}$ to 0.5	V
$V_{IN}$	DC Input Voltage	-0.5	7.0	V
$I_{IK}$	DC Input Diode Current		-50	mA
	$V_{IN} < 0$ V			
$I_{OUT}$	DC Output Sink Current		128	mA
$I_{CC}$ or $I_{GND}$	DC $V_{CC}$ or Ground Current		±100	mA
$T_{STG}$	Storage Temperature Range	-65	+150	°C
$T_J$	Junction Temperature Under Bias		+150	°C
$T_L$	Junction Lead Temperature (Soldering, 10 Seconds)		+260	°C
$P_D$	Power Dissipation at +85°C	SOT-23	200	mW
		SC70-5	150	
ESD	Human Body Model, JEDEC:JESD22-A114		4000	V
	Charge Device Model: JEDEC:JESD22-C101		1500	

### Note:

- The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

## Recommended Operating Conditions

The Recommended Operating Conditions table defines the conditions for actual device operation. Recommended operating conditions are specified to ensure optimal performance to the datasheet specifications. Fairchild does not recommend exceeding them or designing to Absolute Maximum Ratings.

Symbol	Parameter	Conditions	Min.	Max.	Unit
$V_{CC}$	Supply Voltage Operating		1.65	5.50	V
$V_{IN}$	Input Voltage		0	5.5	V
$V_S$	Switch Input Voltage		0	$V_{CC}$	V
$V_{OUT}$	Output Voltage		0	$V_{CC}$	V
$t_r, t_f$	Input Rise and Fall Times	$V_{CC}=2.3$ V - 3.6 V	0	10	ns/V
		$V_{CC}=4.5$ V - 5.5 V	0	5	
		Switching I/O	0	DC	
$T_A$	Operating Temperature		-40	+85	°C
$\theta_{JA}$	Thermal Resistance	SOT-23		300	°C/W
		SC70-5		425	

### Note:

- Unused inputs must be held HIGH or LOW; they may not float.

## DC Electrical Characteristics

All typical values are at the specified  $V_{CC}$ , and  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	$V_{CC}$	Conditions	$T_A = -40$ to $+85^\circ\text{C}$			$T_A = +25^\circ\text{C}$		Units
				Min.	Typ.	Max.	Min.	Typ.	
$V_{IH}$	HIGH Level Input Voltage	1.65 to 1.95		$0.75 V_{CC}$					V
		2.30 to 5.50		$0.7 V_{CC}$					
$V_{IL}$	LOW Level Input Voltage	1.65 to 1.95				$0.25 V_{CC}$			V
		2.30 to 5.50				$0.3 V_{CC}$			
$I_{IN}$	Control Input Leakage Current	0 to 5.5	$0 \leq V_{IN} \leq 5.5 \text{ V}$		$\pm 0.05$	$\pm 1.00$			$\mu\text{A}$
$I_{OFF}$	Off Leakage Current	1.65 to 5.50	$0 \leq A, B \leq V_{CC}$		$\pm 0.05$	$\pm 10.00$			$\mu\text{A}$
$R_{ON}$	Switch On Resistance <sup>(3)</sup>	4.5	$V_{IN}=0 \text{ V}, I_{IN}=30 \text{ mA}$		3	7			$\Omega$
			$V_{IN}=2.4 \text{ V}, I_{IN}=15 \text{ mA}$		5	12			
			$V_{IN}=4.5 \text{ V}, I_{IN}=30 \text{ mA}$		7	15			
		3.0	$V_{IN}=0 \text{ V}, I_{IN}=24 \text{ mA}$		4	9			
			$V_{IN}=3 \text{ V}, I_{IN}=24 \text{ mA}$		10	20			
		2.30	$V_{IN}=0 \text{ V}, I_{IN}=8 \text{ mA}$		5	12			
			$V_{IN}=2.3 \text{ V}, I_{IN}=8 \text{ mA}$		13	30			
		1.8	$V_{IN}=0 \text{ V}, I_{IN}=4 \text{ mA}$		7	28			
$V_{IN}=1.8 \text{ V}, I_{IN}=4 \text{ mA}$			25	60					
$R_{flat}$	On Resistance Flatness <sup>(3,4,5)</sup>	5.0	$I_A = -30 \text{ mA}, 0 \leq V_{Bn} \leq V_{CC}$					6	$\Omega$
		3.3	$I_A = -24 \text{ mA}, 0 \leq V_{Bn} \leq V_{CC}$					12	
		2.5	$I_A = -8 \text{ mA}, 0 \leq V_{Bn} \leq V_{CC}$					28	
		1.8	$I_A = -4 \text{ mA}, 0 \leq V_{Bn} \leq V_{CC}$					125	
$I_{CC}$	Quiescent Supply Current	1.65 to 5.50	$V_{IN} = V_{CC}$ or $\text{GND}, I_{OUT}=0$		0.05	10.00			$\mu\text{A}$

### Notes:

- Measured by the voltage drop between pins A and B at the indicated current through the switch. On resistance is determined by the lower of the voltages on the two (A or B) pins.
- Parameter is characterized but not tested in production.
- Flatness is defined as the difference between the maximum and minimum value of on resistance over the specified range of conditions.

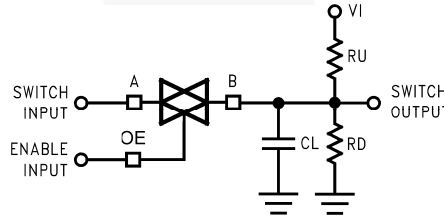
## AC Electrical Characteristics

All typical values are at the specified  $V_{CC}$ , and  $T_A = 25^\circ\text{C}$ .

Symbol	Parameter	$V_{CC}$	Conditions	$T_A = -40 \text{ to } +85^\circ\text{C}$ , $C_L = 50\text{Pf}$ , $R_U = R_D = 500 \Omega$			Units	Figure
				Min.	Typ.	Max.		
$t_{PHL}, t_{PLH}$	Propagation Delay Bus-to-Bus <sup>(6)</sup>	1.65 to 1.95	$V_{IN} = \text{OPEN}$			4.3	ns	Figure 5 Figure 6
		2.3 to 2.7				1.2		
		3.0 to 3.6				0.8		
		4.5 to 5.5				0.3		
$t_{PZL}, t_{PZH}$	Output Enable Time	1.65 to 1.95	$V_{IN} = 2 \times V_{CC}$ for $t_{PZL}$ , $V_{IN} = 0 \text{ V}$ for $t_{PZH}$	1.5	7.0	14.2	ns	Figure 5 Figure 6
		2.3 to 2.7		1.5	3.3	7.0		
		3.0 to 3.6	1.5	2.4	5.5			
		4.5 to 5.5	1.5	2.0	4.5			
$t_{PLZ}, t_{PHZ}$	Output Disable Time	1.65 to 1.95	$V_{IN} = 2 \times V_{CC}$ for $t_{PLZ}$ , $V_{IN} = 0 \text{ V}$ for $t_{PHZ}$	1.5	9.2	18.2	ns	Figure 5 Figure 6
		2.3 to 2.7		1.5	5.3	9.0		
		3.0 to 3.6	1.5	4.0	7.0			
		4.5 to 5.5	1.5	2.7	5.0			
$C_{IN}$	Control Pin Input Capacitance		$V_{CC} = 0$		2		pF	
$C_{I/O}$	Input / Output Capacitance		$V_{CC} = 05.0 \text{ V}$		6		pF	

**Note:**

6. This parameter is guaranteed by design but is not tested. The switch contributes no propagation delay other than the RC delay of the typical on resistance of the switch and the 50pF load capacitance, when driven by an ideal voltage source (zero output impedance).



**Notes:**

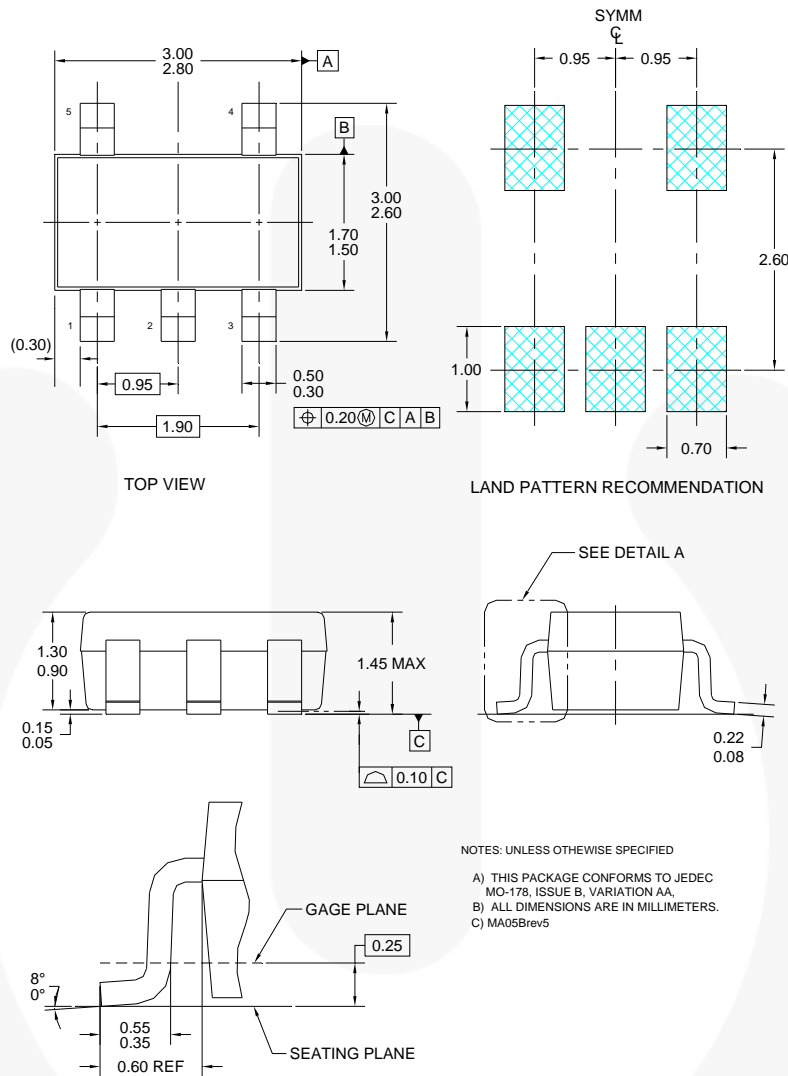
- Input driven by 50  $\Omega$ ; source terminated in 50  $\Omega$ .
- $C_L$  includes load and stray capacitance.
- Input PRR=1.0 MHz;  $t_w=500 \text{ ns}$ .

Figure 4. AC Test Circuit



Figure 5. AC Waveforms

## Physical Dimensions



**Figure 6. 5-Lead SOT23, JEDEC MO-178 1.6 mm**

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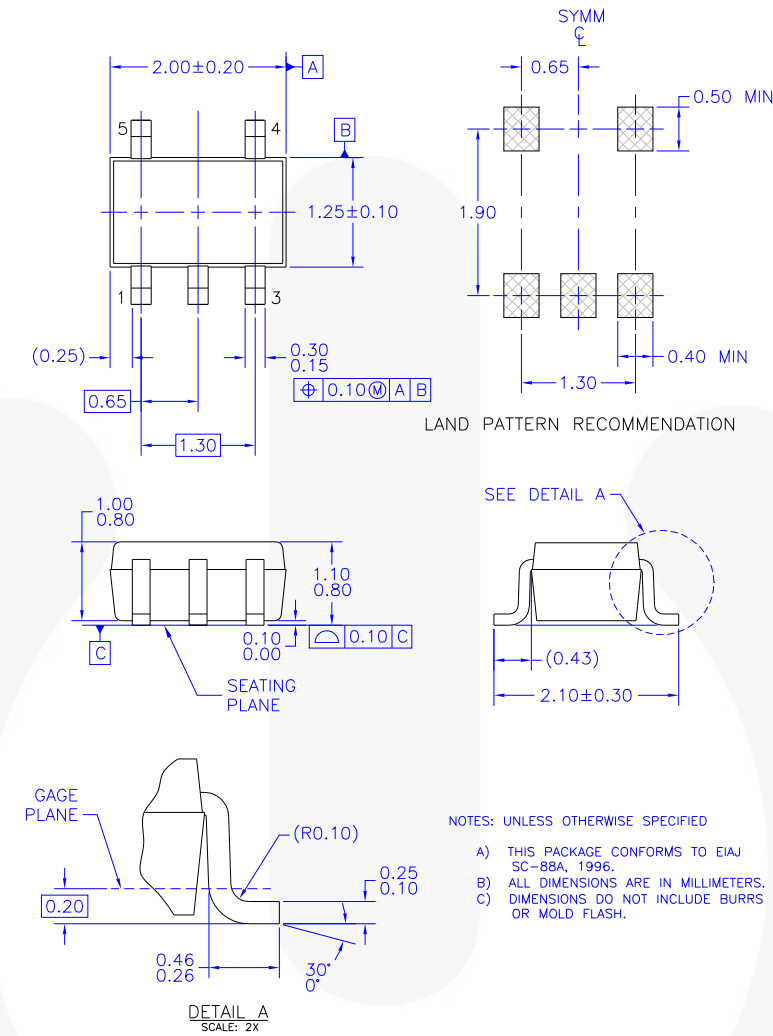
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## Tape and Reel Specifications

Please visit Fairchild Semiconductor's online packaging area for the most recent tape and reel specifications:  
[http://www.fairchildsemi.com/packaging/SOT23-5L\\_tr.pdf](http://www.fairchildsemi.com/packaging/SOT23-5L_tr.pdf).

Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
M5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed

## Physical Dimensions



MAA05AREV5

**Figure 7. 5-Lead, SC70, EIAJ SC-88a, 1.25 mm Wide**

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Package Designator	Tape Section	Cavity Number	Cavity Status	Cover Type Status
P5X	Leader (Start End)	125 (Typical)	Empty	Sealed
	Carrier	3000	Filled	Sealed
	Trailer (Hub End)	75 (Typical)	Empty	Sealed







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